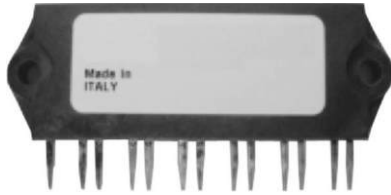


IGBT SIP Module (Short Circuit Rated Ultrafast IGBT)


IMS-2
FEATURES

- Short circuit rated ultrafast: Optimized for high speed > 5.0 kHz, and short circuit rated to 10 μ s at 125 °C, $V_{GE} = 15$ V
- Fully isolated printed circuit board mount package
- Switching-loss rating includes all “tail” losses
- HEXFRED® soft ultrafast diodes
- Totally lead (Pb)-free and RoHS compliant
- Designed and qualified for industrial level


**RoHS
COMPLIANT**
PRODUCT SUMMARY
OUTPUT CURRENT IN A TYPICAL 20 kHz MOTOR DRIVE

I_{RMS} per phase (3.1 kW total) with $T_C = 90$ °C	11 A_{RMS}
T_J	125 °C
Supply voltage	360 Vdc
Power factor	0.8
Modulation depth (see fig. 1)	115 %
$V_{CE(on)}$ (typical) at $I_C = 13$ A, 25 °C	1.8 V

DESCRIPTION

The IGBT technology is the key to Vishay’s HPP advanced line of IMS (Insulated Metal Substrate) power modules. These modules are more efficient than comparable bipolar transistor modules, while at the same time having the simpler gate-drive requirements of the familiar power MOSFET. This superior technology has now been coupled to a state of the art materials system that maximizes power throughput with low thermal resistance. This package is highly suited to motor drive applications and where space is at a premium.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Collector to emitter voltage	V_{CES}		600	V
Continuous collector current	I_C	$T_C = 25$ °C	24	A
		$T_C = 100$ °C	13	
Pulsed collector current	$I_{CM}^{(1)}$		48	
Clamped inductive load current	$I_{LM}^{(2)}$		48	
Short circuit withstand time	t_{SC}	$T_C = 100$ °C	9.3	μ s
Gate to emitter voltage	V_{GE}		± 20	V
Isolation voltage	V_{ISOL}	t = 1 min, any terminal to case	2500	V_{RMS}
Maximum power dissipation, each IGBT	P_D	$T_C = 25$ °C	63	W
		$T_C = 100$ °C	25	
Operating junction and storage temperature range	T_J, T_{Stg}		- 55 to + 150	°C
Soldering temperature		For 10 s, (0.063" (1.6 mm) from case)	300	
Mounting torque		6-32 or M3 screw	5 to 7 (0.55 to 0.8)	

Notes

(1) Repetitive rating; $V_{GE} = 20$ V, pulse width limited by maximum junction temperature (see fig. 20)

(2) $V_{CC} = 80$ % (V_{CES}), $V_{GE} = 20$ V, L = 10 μ H, $R_G = 10$ Ω (see fig. 19)

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TYP.	MAX.	UNITS
Junction to case, each IGBT, one IGBT in conduction	R_{thJC} (IGBT)	-	2.2	°C/W
Junction to case, each DIODE, one DIODE in conduction	R_{thJC} (DIODE)	-	3.7	
Case to sink, flat, greased surface	R_{thCS} (MODULE)	0.10	-	
Weight of module		20	-	g
		0.7	-	oz.

ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Collector to emitter breakdown voltage	$V_{(BR)CES}^{(1)}$	$V_{GE} = 0\text{ V}, I_C = 250\text{ }\mu\text{A}$		600	-	-	V
Temperature coeff. of breakdown voltage	$\Delta V_{(BR)CES}/\Delta T_J$	$V_{GE} = 0\text{ V}, I_C = 1.0\text{ mA}$		-	0.63	-	V/°C
Collector to emitter saturation voltage	$V_{CE(on)}$	$I_C = 13\text{ A}$	$V_{GE} = 15\text{ V}$ See fig. 2, 5	-	1.80	2.3	V
		$I_C = 24\text{ A}$		-	1.80	-	
		$I_C = 13\text{ A}, T_J = 150\text{ }^\circ\text{C}$		-	1.56	1.73	
Gate threshold voltage	$V_{GE(th)}$	$V_{CE} = V_{GE}, I_C = 250\text{ }\mu\text{A}$		3.0	-	6.0	mV/°C
Temperature coeff. of threshold voltage	$\Delta V_{GE(th)}/\Delta T_J$			-	-13	-	
Forward transconductance	$g_{fe}^{(2)}$	$V_{CE} = 100\text{ V}, I_C = 10\text{ A}$		11	18	-	S
Zero gate voltage collector current	I_{CES}	$V_{GE} = 0\text{ V}, V_{CE} = 600\text{ V}$		-	-	250	μA
		$V_{GE} = 0\text{ V}, V_{CE} = 600\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	3500	
Diode forward voltage drop	V_{FM}	$I_C = 15\text{ A}$	See fig. 13	-	1.3	1.7	V
		$I_C = 15\text{ A}, T_J = 150\text{ }^\circ\text{C}$		-	1.2	1.6	
Gate to emitter leakage current	I_{GES}	$V_{GE} = \pm 20\text{ V}$		-	-	± 100	nA

Notes

(1) Pulse width $\leq 80\text{ }\mu\text{s}$, duty factor $\leq 0.1\%$

(2) Pulse width $5.0\text{ }\mu\text{s}$; single shot



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SWITCHING CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS	
Total gate charge (turn-on)	Q_g	$I_C = 13\text{ A}$		-	110	170	nC	
Gate to emitter charge (turn-on)	Q_{ge}	$V_{CC} = 400\text{ V}$		-	14	21		
Gate to collector charge (turn-on)	Q_{gc}	$V_{GE} = 15\text{ V}$ See fig. 8		-	49	74		
Turn-on delay time	$t_{d(on)}$	$T_J = 25\text{ }^\circ\text{C}$ $I_C = 13\text{ A}, V_{CC} = 480\text{ V}$ $V_{GE} = 15\text{ V}, R_G = 10\text{ }\Omega$ Energy losses include "tail" and diode reverse recovery See fig. 9, 10, 18		-	50	-	ns	
Rise time	t_r			-	30	-		
Turn-off delay time	$t_{d(off)}$			-	110	170		
Fall time	t_f			-	91	140		
Turn-on switching loss	E_{on}			-	0.56	-		mJ
Turn-off switching loss	E_{off}	-	0.28	-				
Total switching loss	E_{ts}	-	0.84	1.1				
Short circuit withstand time	t_{sc}	$V_{CC} = 360\text{ V}, T_J = 125\text{ }^\circ\text{C}$ $V_{GE} = 15\text{ V}, R_G = 10\text{ }\Omega, V_{CPK} < 500\text{ V}$		10	-	-	μs	
Turn-on delay time	$t_{d(on)}$	$T_J = 150\text{ }^\circ\text{C}$, see fig. 9, 10, 11, 18 $I_C = 13\text{ A}, V_{CC} = 480\text{ V}$ $V_{GE} = 15\text{ V}, R_G = 10\text{ }\Omega$ Energy losses include "tail" and diode reverse recovery		-	47	-	ns	
Rise time	t_r			-	30	-		
Turn-off delay time	$t_{d(off)}$			-	250	-		
Fall time	t_f			-	150	-		
Total switching loss	E_{ts}			-	1.28	-		mJ
Internal emitter inductance	L_E	Measured 5 mm from package		-	7.5	-	nH	
Input capacitance	C_{ies}	$V_{GE} = 0\text{ V}$		-	1600	-	pF	
Output capacitance	C_{oes}	$V_{CC} = 30\text{ V}$ $f = 1.0\text{ MHz}$		-	130	-		
Reverse transfer capacitance	C_{res}	See fig. 7		-	55	-		
Diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$	See fig. 14	$I_F = 15\text{ A}$ $V_R = 200\text{ V}$ $dI/dt = 200\text{ A}/\mu\text{s}$	-	42	60	ns
		$T_J = 125\text{ }^\circ\text{C}$			-	74	120	
Diode peak reverse recovery charge	I_{rr}	$T_J = 25\text{ }^\circ\text{C}$	See fig. 15		-	4.0	6.0	A
		$T_J = 125\text{ }^\circ\text{C}$			-	6.5	10	
Diode reverse recovery charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}$	See fig. 16		-	80	180	nC
		$T_J = 125\text{ }^\circ\text{C}$			-	220	600	
Diode peak rate of fall of recovery during t_b	$dI_{(rec)M}/dt$	$T_J = 25\text{ }^\circ\text{C}$	See fig. 17		-	188	-	A/ μs
		$T_J = 125\text{ }^\circ\text{C}$		-	160	-		

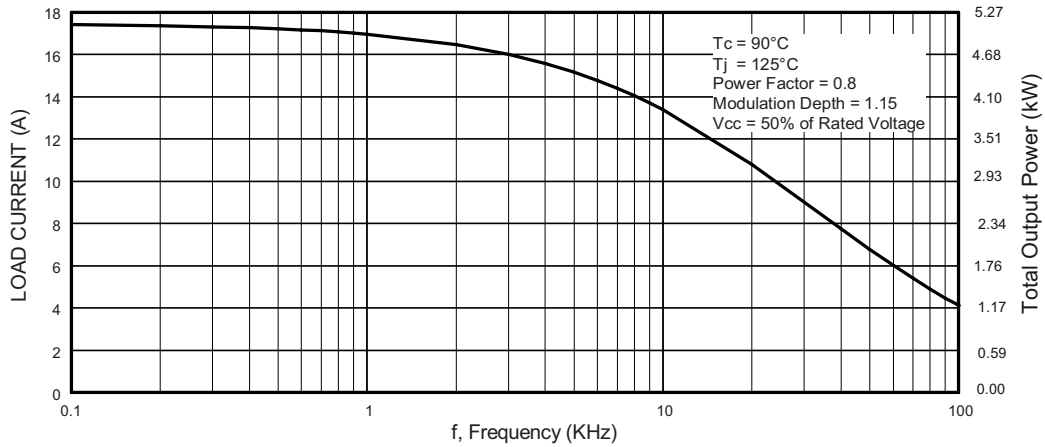


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of Fundamental)

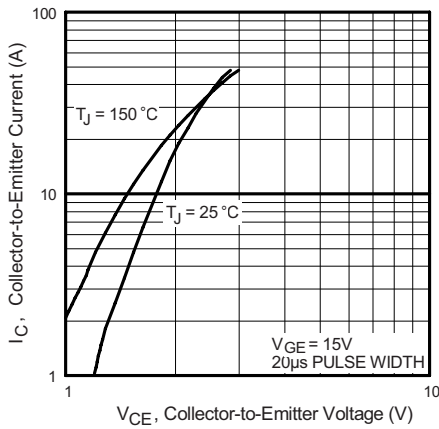


Fig. 2 - Typical Output Characteristics

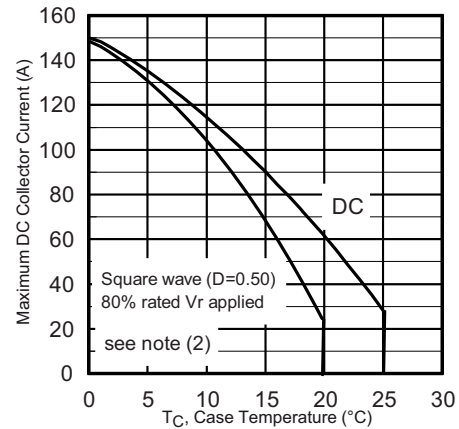


Fig. 4 - Maximum Collector Current vs. Case Temperature

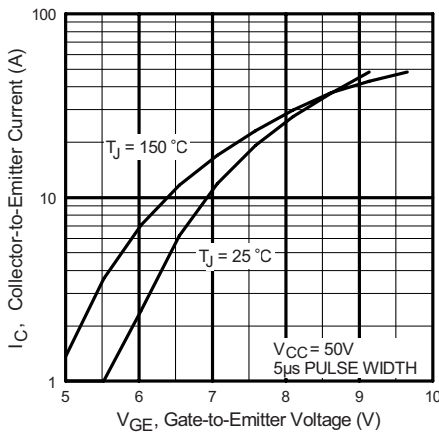


Fig. 3 - Typical Output Characteristics

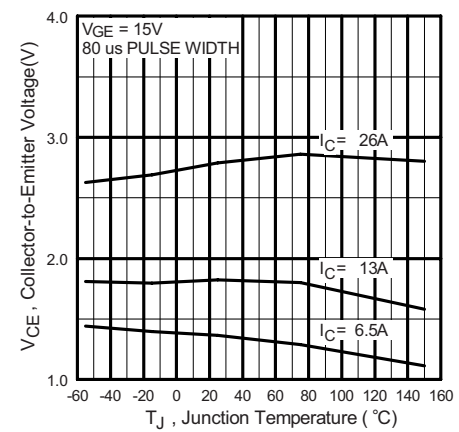


Fig. 5 - Typical Collector to Emitter Voltage vs. Junction Temperature

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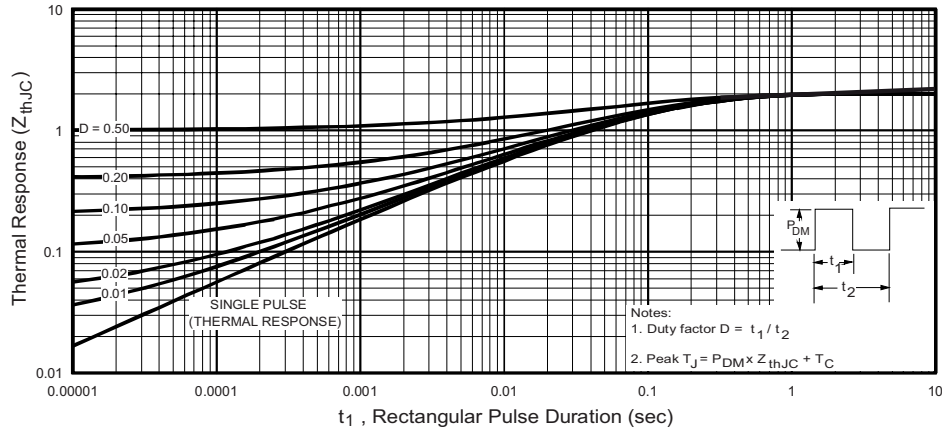


Fig. 6 - Maximum IGBT Effective Transient Thermal Impedance, Junction to Case

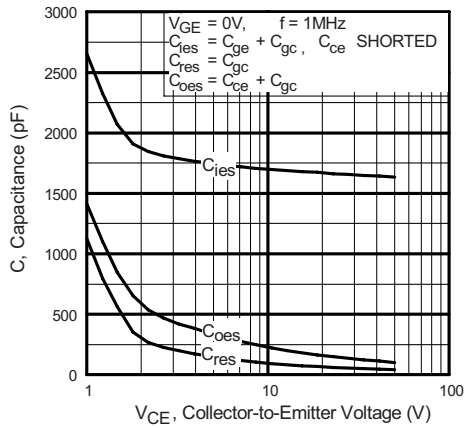


Fig. 7 - Typical Capacitance vs. Collector to Emitter Voltage

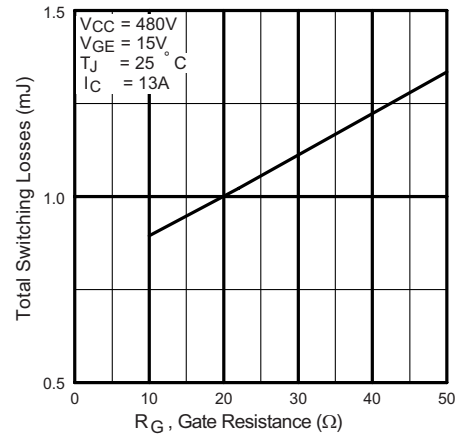


Fig. 9 - Typical Switching Losses vs. Gate Resistance

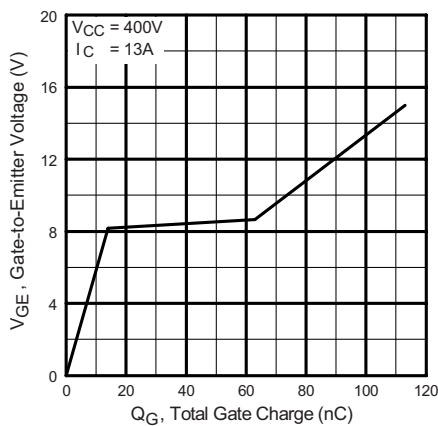


Fig. 8 - Typical Gate Charge vs. Gate to Emitter Voltage

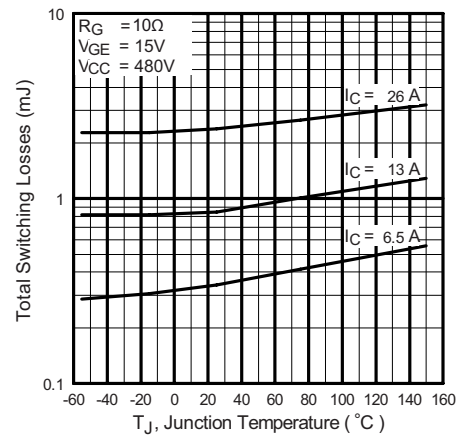


Fig. 10 - Typical Switching Losses vs. Junction Temperature

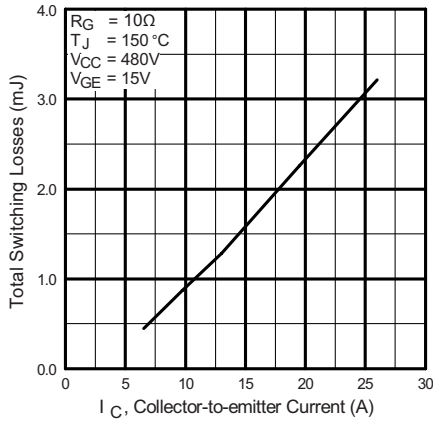


Fig. 11 - Typical Switching Losses vs. Collector to Emitter Current

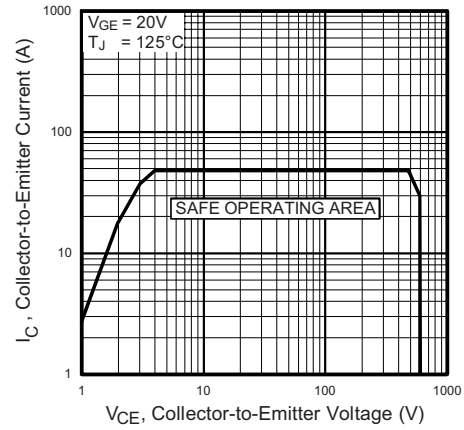


Fig. 12 - Turn-Off SOA

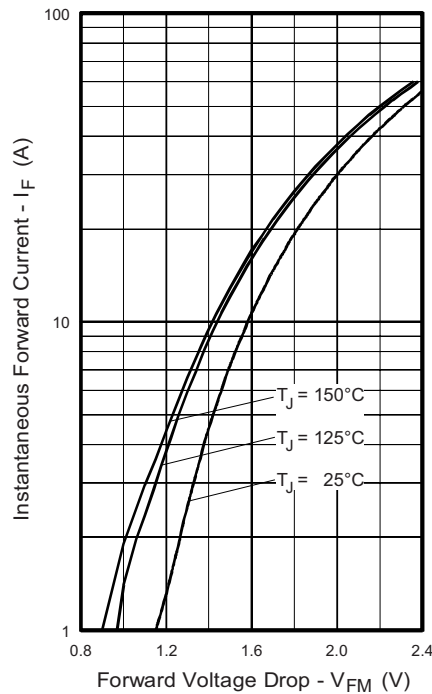


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

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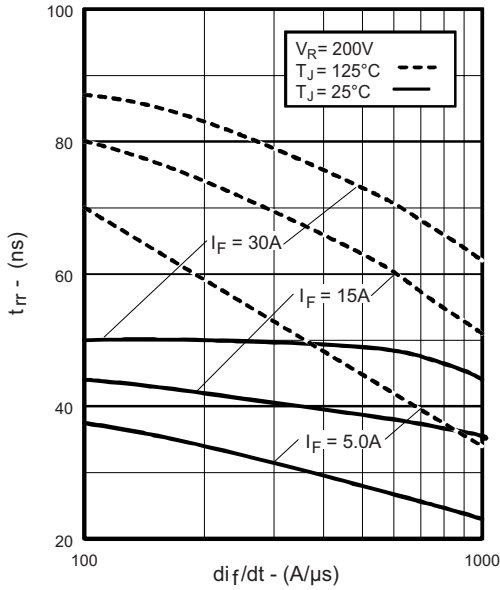


Fig. 14 - Typical Reverse Recovery Time vs. di_F/dt

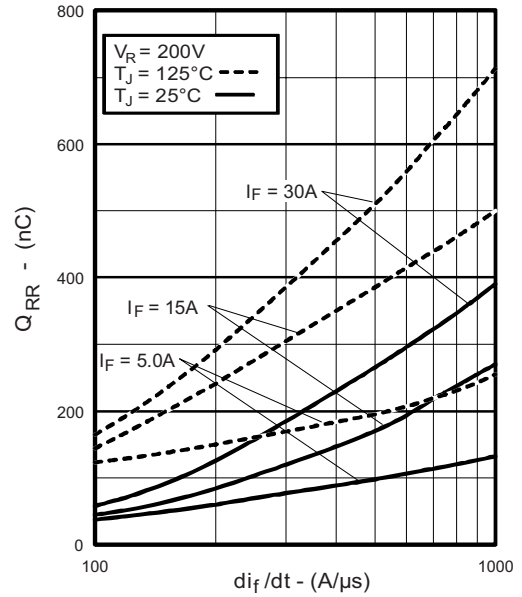


Fig. 16 - Typical Stored Charge vs. di_F/dt

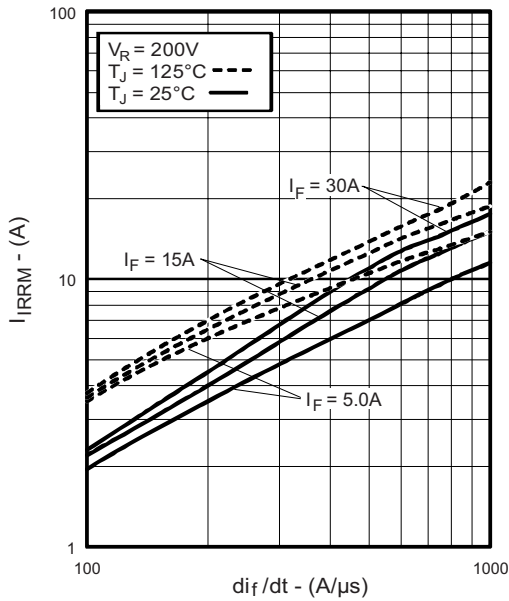


Fig. 15 - Typical Recovery Current vs. di_F/dt

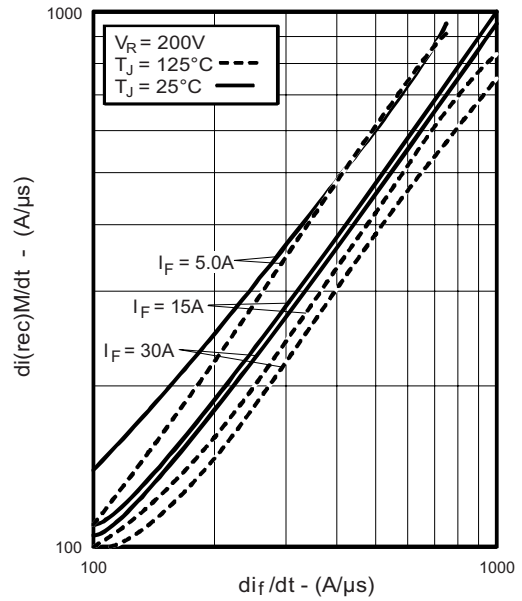


Fig. 17 - Typical $dI_{(rec)M}/dt$ vs di_F/dt

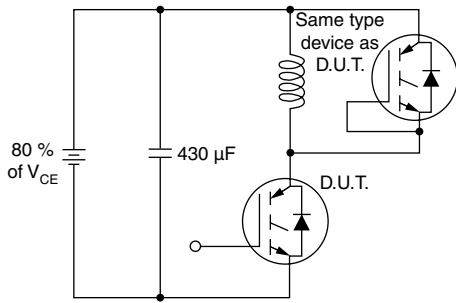


Fig. 18a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off}(\text{diode})$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

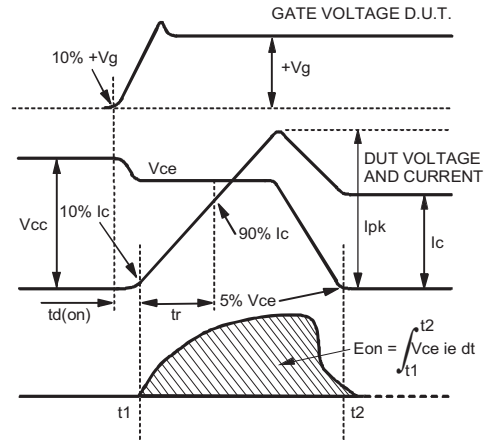


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

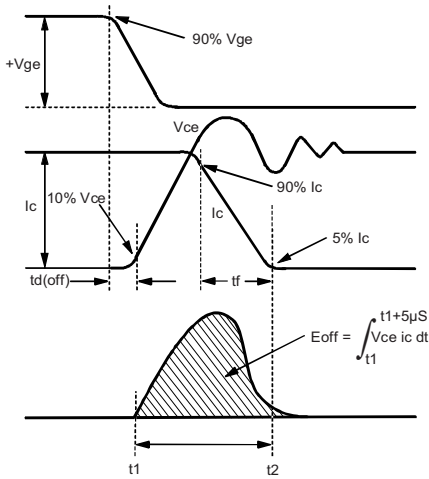


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

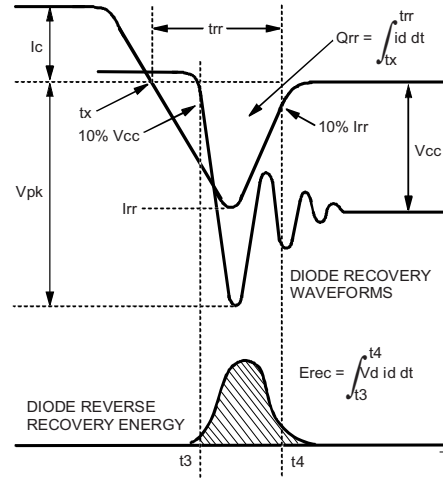


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

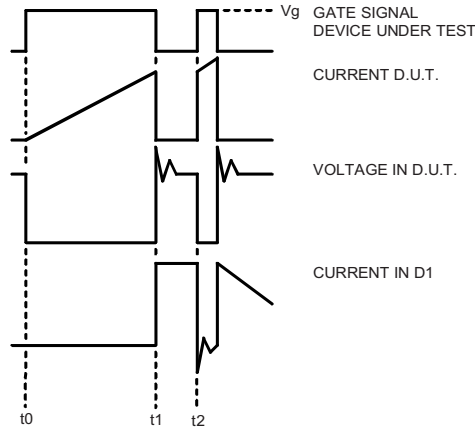


Fig. 18e - Macro Waveforms for Figure 18a's Test Circuit

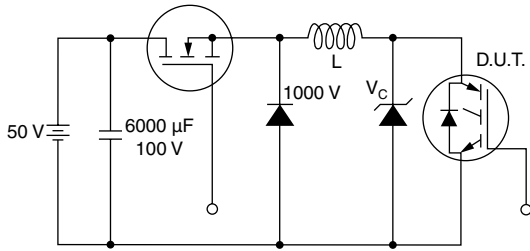


Fig. 19 - Clamped Inductive Load Test Circuit

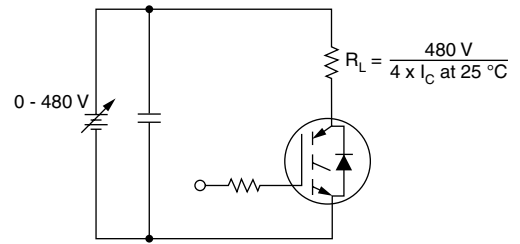
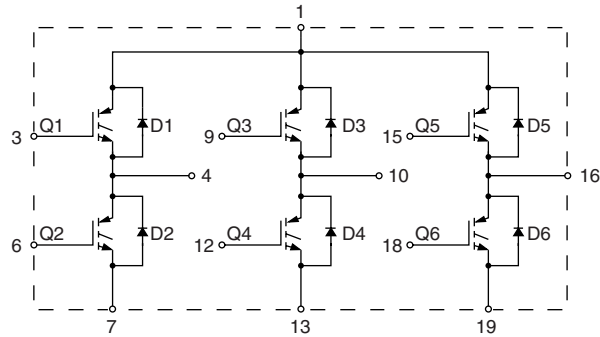


Fig. 20 - Pulsed Collector Current Test Circuit

CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95066



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